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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year II Semester Regular Examinations November-2021
ALGORITHMS FOR VLSI DESIGN AUTOMATION

Time: 3 hours

Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

- 1 Explain about the design methodology based on top-down structural decomposition and bottom up Layout reconstruction using Gajski's y-chart. **L2 12M**

OR

- 2 a How combinational optimization is achieved using Local and Tabu search? **L3 6M**
b Explain the following: (i) Backtracking. (ii) Branch and bound programming. **L1 6M**

UNIT-II

- 3 a With an example, explain the difference between modeling and simulation. **L1 6M**
b Explain Gate level and switch level modeling. **L2 6M**

OR

- 4 What is meant by modeling and simulation? Differentiate gate level and switch level modeling and simulation procedures with suitable example **L2 12M**

UNIT-III

- 5 Explain Heuristic based on ROBDD? **L2 12M**

OR

- 6 a What is a combinational logic synthesis? **L2 6M**
b With practical example explain the combinational logic synthesis? **L3 6M**

UNIT-IV

- 7 Explain the following algorithms **L1 6M**
a ASAP algorithm.
b Mobility based scheduling. **L1 6M**

OR

- 8 With detailed example explain the allocation, assignment and scheduling **L3 12M**

UNIT-V

- 9 a With neat sketch explain about the physical design cycle of MCM. **L3 6M**
b Briefly explain about the different approaches to be followed for General MCM routing problems. **L1 6M**

OR

- 10 a Explain the FPGA technologies. **L2 6M**
b How partitioning is performed for segmented model. **L3 6M**

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